CONCLUSIVE ENGINEERING

WHLE-LS1 Datasheet

Version 2.1

- NXP LS1 Series SoC
- DPAA/DPAA2
- PCI Express
- USB 3.0 host mode
- USB 2.0 device mode
- DDR4 Memory
- eMMC Storage
- 2 x 10Gbit/s SFP+
- 4 x 1Gbit/s RJ45

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2. Revision history

Table 2.1 Revision History

Revision	Date	Notes
1.0	2022-03-08	Initial - Preliminary
1.1	2022-05-12	Review and detailed update of all sections
1.2	2022-05-31	Added EEPROM accessibility over I2C and PCIe version on M.2
1.3	2024-01-05	Update to version 2.1

3. Overview

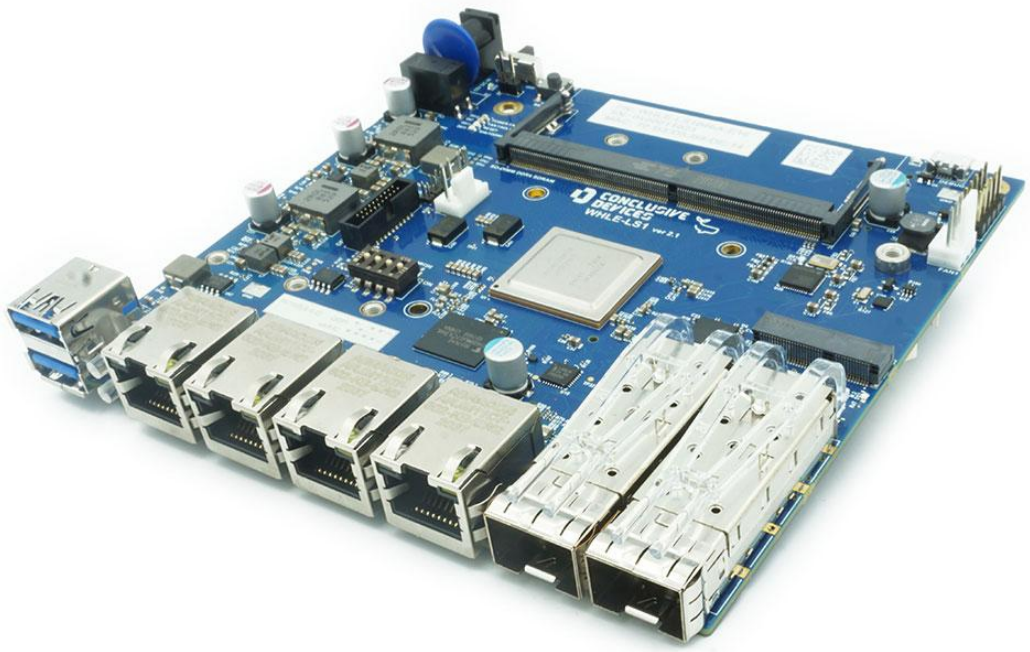


Fig. 3.1 WHLE-LS1 board overview

The Conclusive Engineering Whale WHLE-LS1 is a series of high-performance Single Board Computers. They are powered by the NXP QorIQ® Layerscape® SoC series, available in variants optimized for efficiency (based on ARM® Cortex®-A53) or computation power (based on ARM® Cortex®-A72). The SoC range is capable of delivering an approximate performance from 15,000 to 45,000 CoreMark.

WHLE-LS1 offers features typically associated with SmartNICs thanks to Layerscape's integrated Data Path Acceleration Architecture, fully leveraged in board design. It offers fine-grained control over its 6 Ethernet connectors (4xRJ45, 2xSFP+) and advanced traffic routing and processing capabilities.

WHLE-LS1 is capable of native, hardware-supported real time operation.

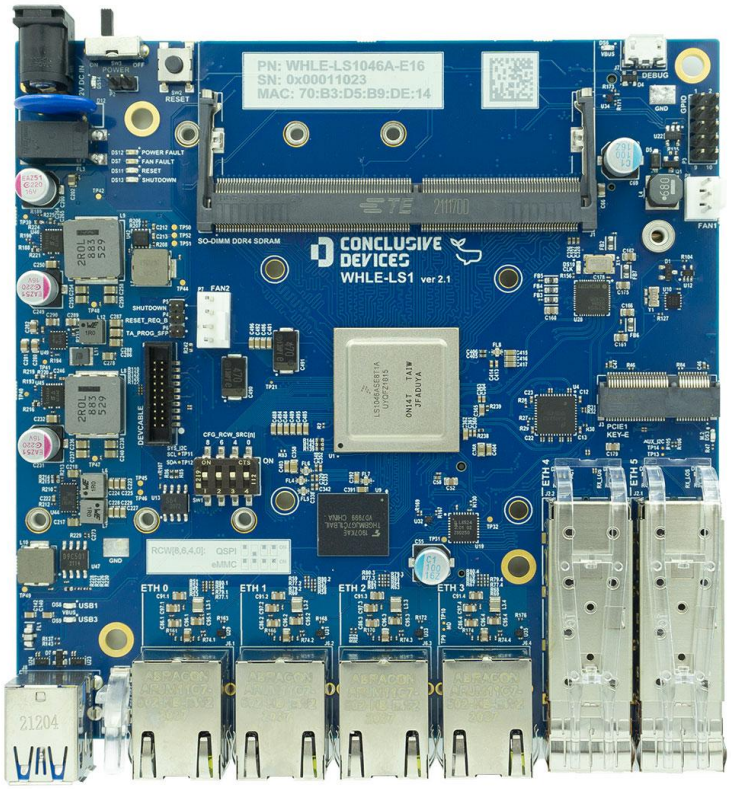


Fig. 3.2 WHLE-LS1 board TOP view

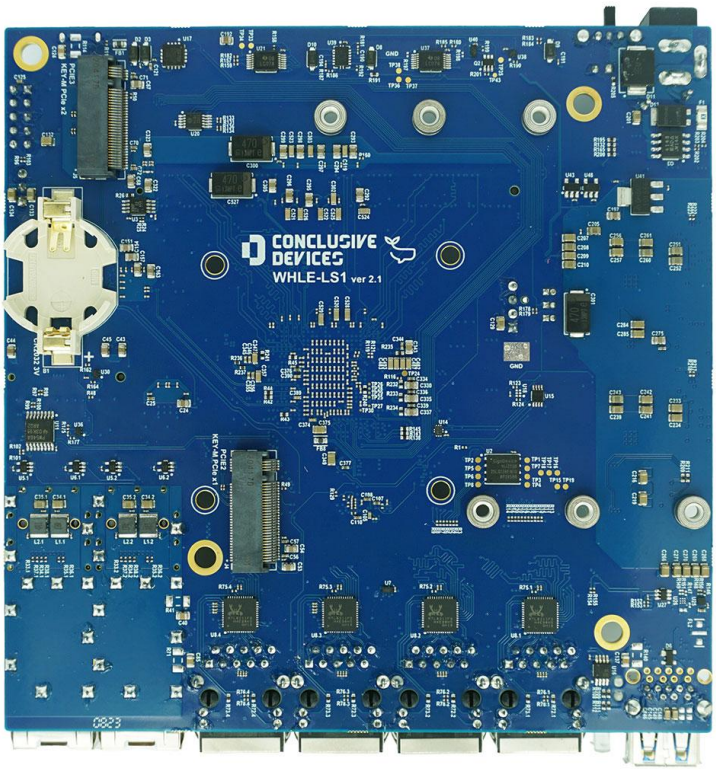


Fig. 3.3 WHLE-LS1 board BOTTOM view

4. Features of WHLE-LS1

- NXP QorIQ Layerscape LS10xx SoC:
  - ARM Cortex-A53 or Cortex-A72 cores
  - 2/4/8 core variants
  - Clock up to 1.8GHz
- SODIMM DDR4 slot
  - Supports up to 32GB of SODIMM DDR4 memory
  - ECC support
  - Up to 2.1GT/s
- Connectivity
  - 2 SFP+ interfaces supporting 10000Mbps Ethernet
  - 4 RJ45 interfaces supporting 10/100/1000Mbps Ethernet
- Expansion slots
  - 1 PCIe M.2 x1 Key-E slot
  - 1 PCIe M.2 x1 Key-M slot
  - 1 PCIe M.2 x2 Key-M slot
- Software support
  - Mainline Linux kernel support
  - FreeBSD 13 support (on request)
  - Support for Open Portable Trusted Execution Environment (OP-TEE)
  - Supported Bootloaders:
    - U-Boot
    - UEFI EDK2
    - ARM Trusted Firmware

5. Block Diagram

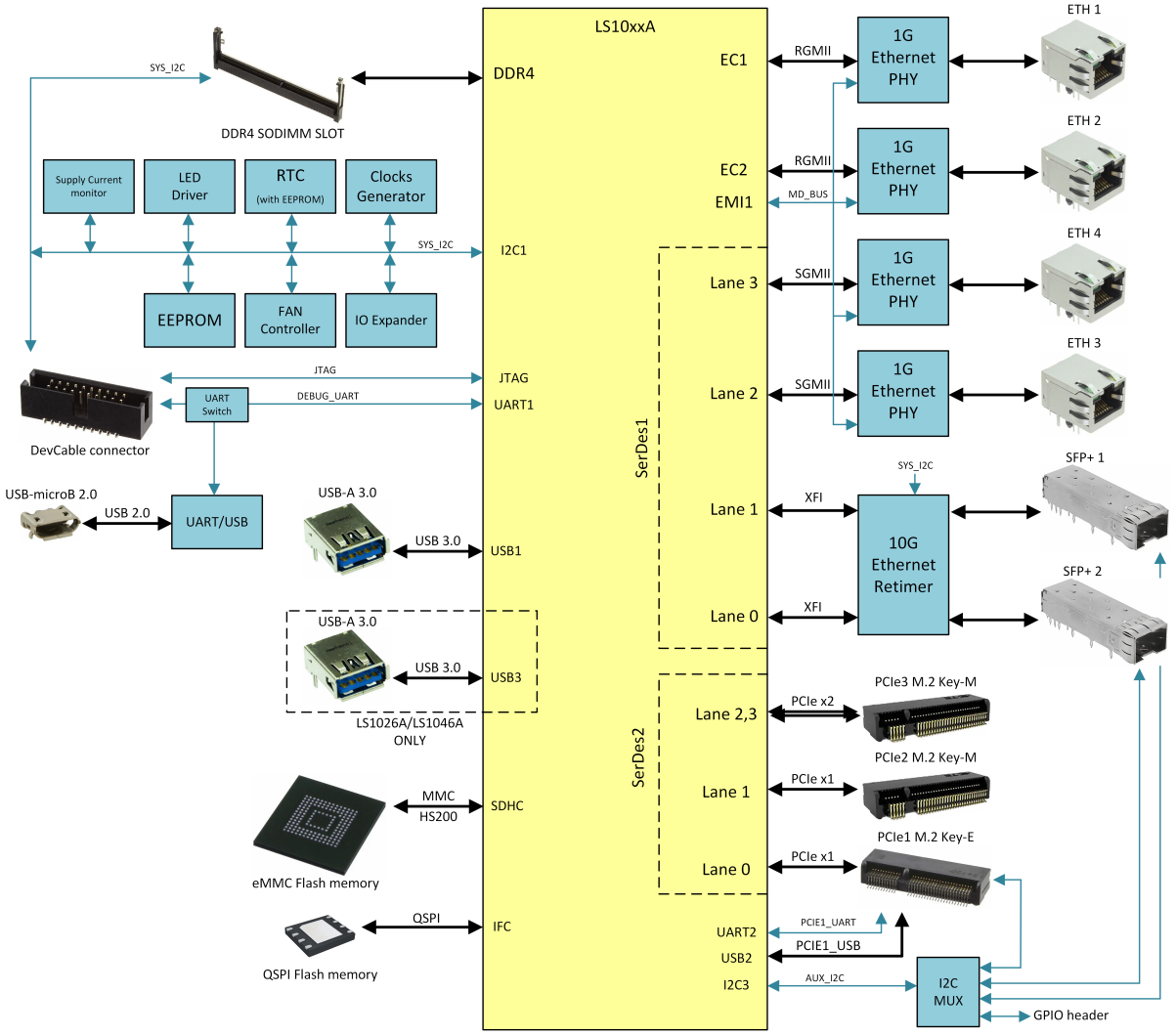
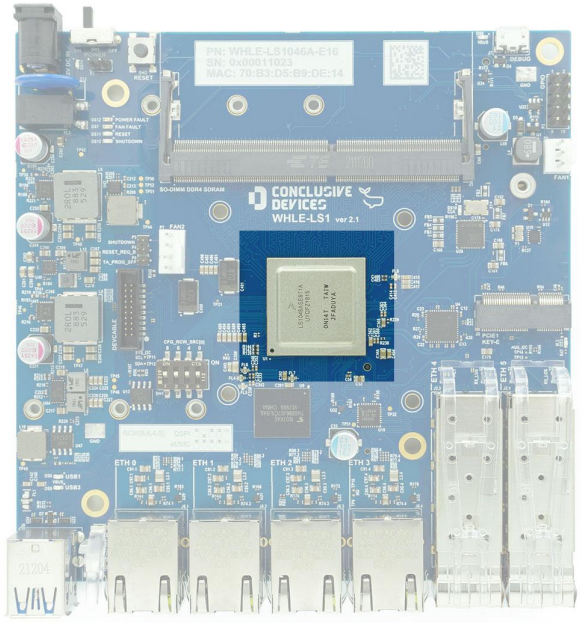


Fig. 5.1 WHLE-LS1 block diagram

6. Main hardware components

This section summarizes the main hardware building blocks of the WHLE-LS1 series single board computer.

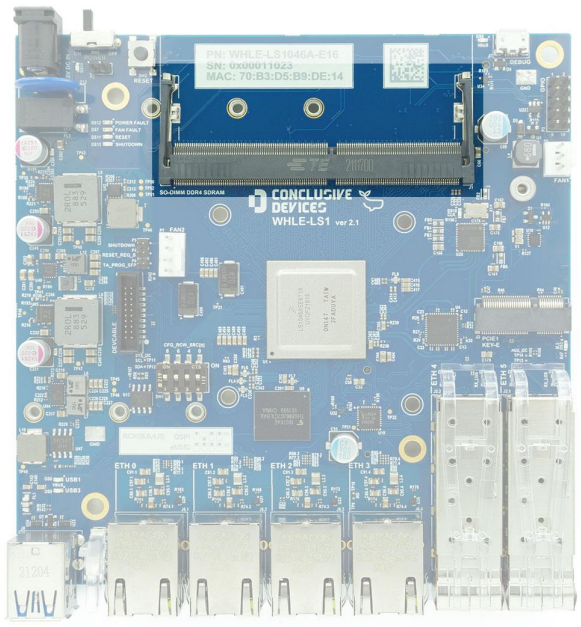
6.1. NXP LS1 Series SoC



- 780 FC-PBGA package, 23 mm x 23 mm
- SoC Available in the following configurations:
  - LS1026A: Dual ARM Cortex-A72 64-bit cores, 2MB L2 cache
  - LS1046A: Quad ARM Cortex-A72 64-bit cores, 2MB L2 cache
  - LS1048A: Quad ARM Cortex-A53 64-bit cores, 1MB L2 cache
  - LS1088A: Octal ARM Cortex-A53 64-bit cores, 2x 1MB L2 cache
- Networking subsystem
  - DPAA (LS1026A, LS1046A)
  - DPAA2 (LS1048A, LS1088A)
- PCI Express interface
  - 3 controllers total, 2 used for internal devices
  - 1 controller available, providing 4 PCIe lanes total for user-attached devices
- USB subsystem
  - USB 3.0 SuperSpeed host

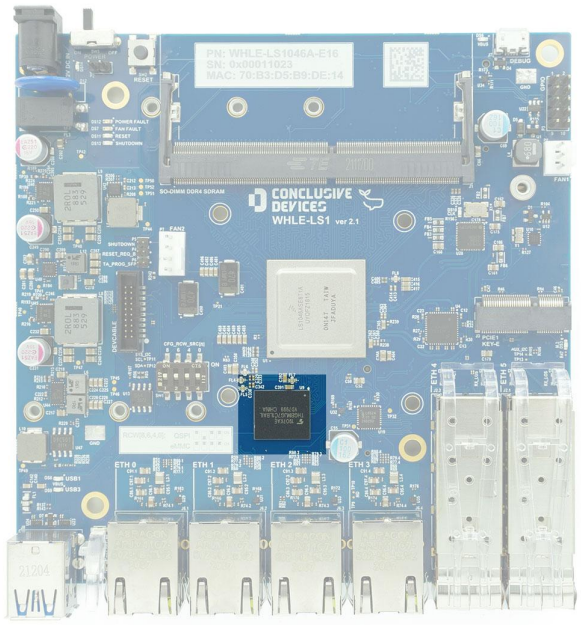
◦ USB 2.0 High Speed device

6.2. DDR4 Memory slot



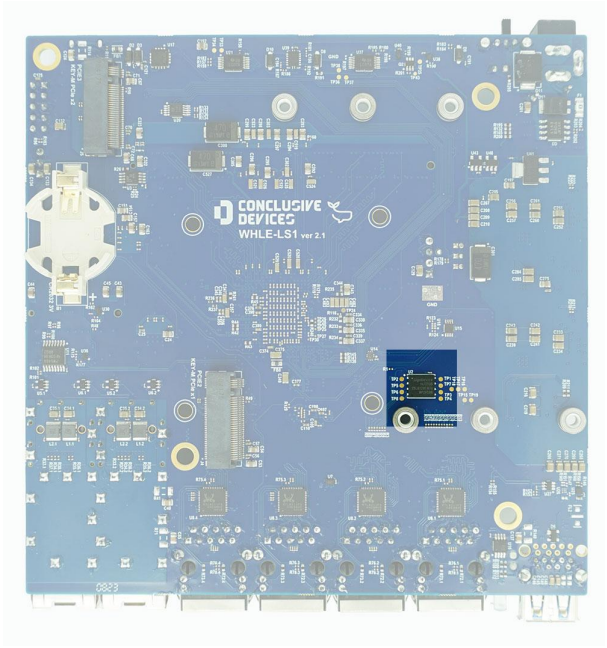
- One SODIMM 260-pin DDR4 slot, attached to the SoC 32/64 bit memory controller.
- Memory controller supports ECC and interleaving
- Transfer speeds up to 2.1GT/s
- Supports SODIMM DDR4 module capacity up to 32GB

6.3. eMMC Storage



- Supports eMMC 4.5 JEDEC standard
- Available capacities:
    - 4GB
    - 16GB
    - 64GB
- RPMB (Replay Protected Memory Block) available for Trusted Execution Environment applications

6.4. QSPI NOR Flash

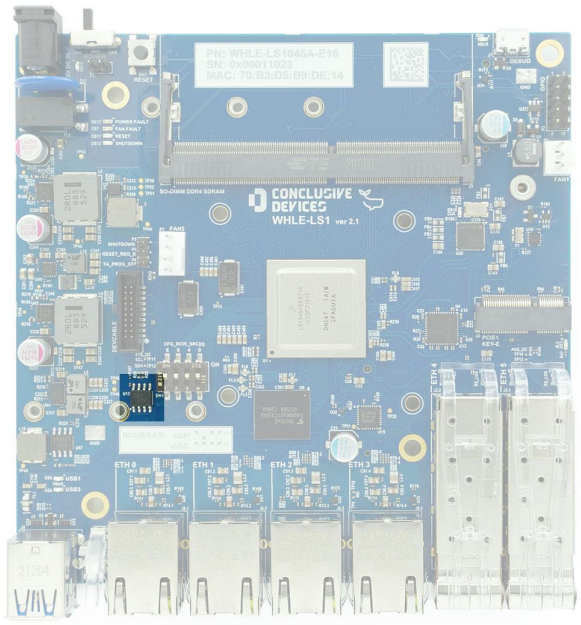


128MB QSPI NOR Flash on the back side of the board. Provides additional fast memory to the LS1 SoC.

- Up to 120MHz read
- Up to 480Mbits/s data transfer
- Typical data retention of 20 years
- 100,000 write/erase cycles (minimum)
- Optimized for fast SoC cache fill

XiP is unsupported.

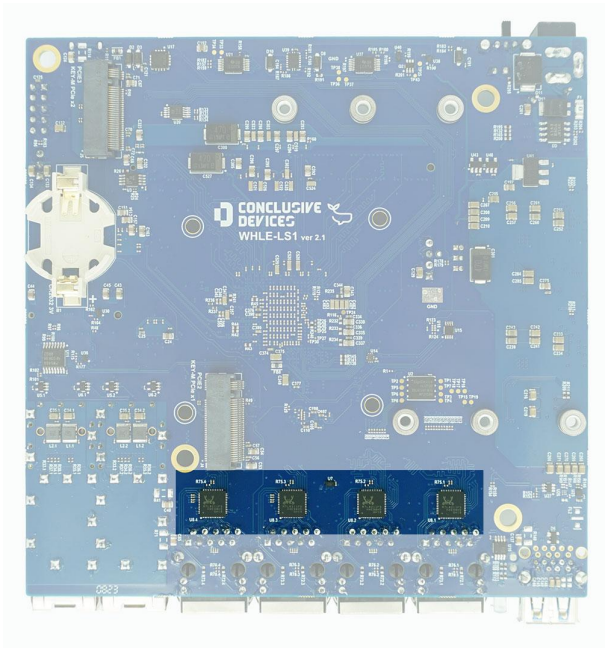
6.5. EEPROM



64Kbit EEPROM (8 blocks of 8Kbit) accessible over I2C.

- Typical page-write cycle time: 2 ms
- Hardware write protection for entire memory
- 1,000,000 erase/write cycles
- Data retention exceeds 200 years

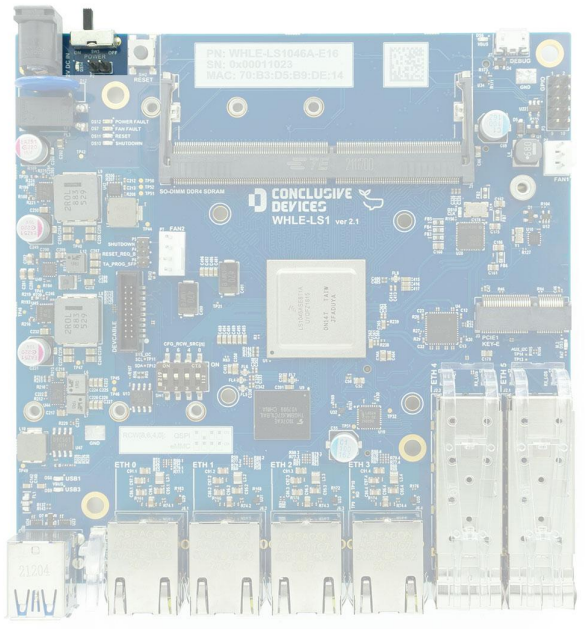
6.6. 10/100/1000Mbit/s Ethernet PHY



Realtek RTL8211FS-CG Ethernet Physical Layer Transceivers on the back side of the board. They control the 4 available Ethernet ports. RTL8211FS-CG provides:

- hardware support for high-precision clock synchronization (based on PTP of IEEE 1588 and 802.1AS).
- crossover detection
- auto-correction
- polarity correction
- adaptive equalization
- cross-talk cancellation
- echo cancellation
- timing recovery
- error correction

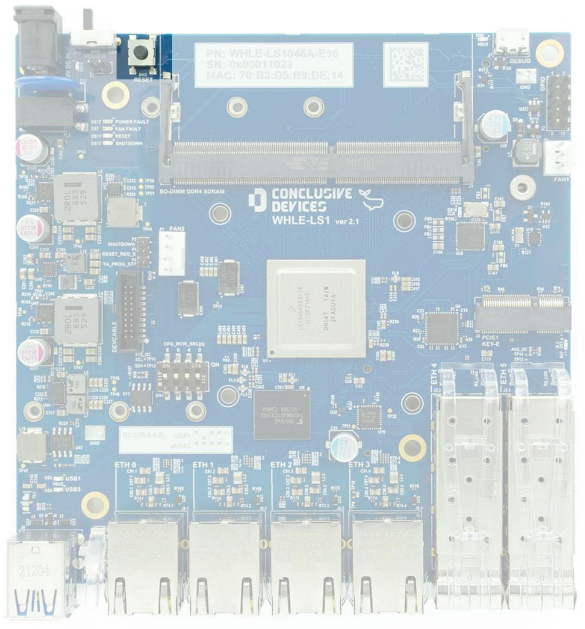
6.7. Power Switch



Power Switch, slide-type. In ON position shorts a signal line that activates the power supply circuit, which begins supplying power to the board components.

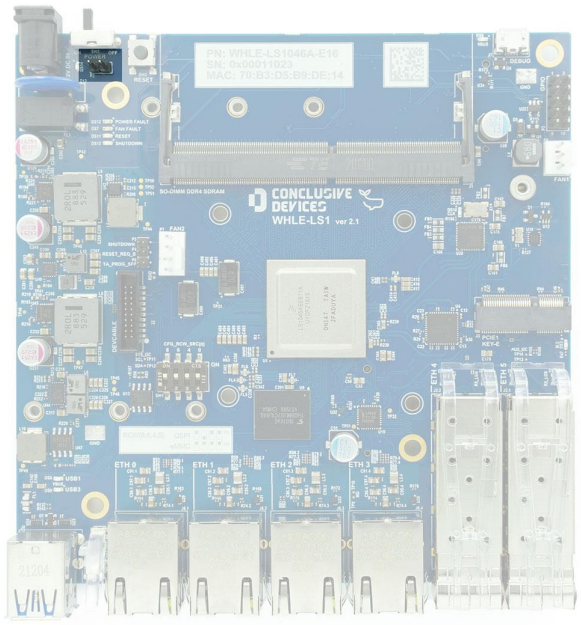
It's internally identical to the Power Switch header pins.

6.8. Reset Button



Pulls the reset button causing a full power cycle of the board. Internally, this causes a power cycle on all power domains, with the exception of VDD_1V8_SHDN and VDD_3V3_SHDN domains which supply power to the board's reset tree and status LEDs. It can be used to wake the SoC from a shutdown state.

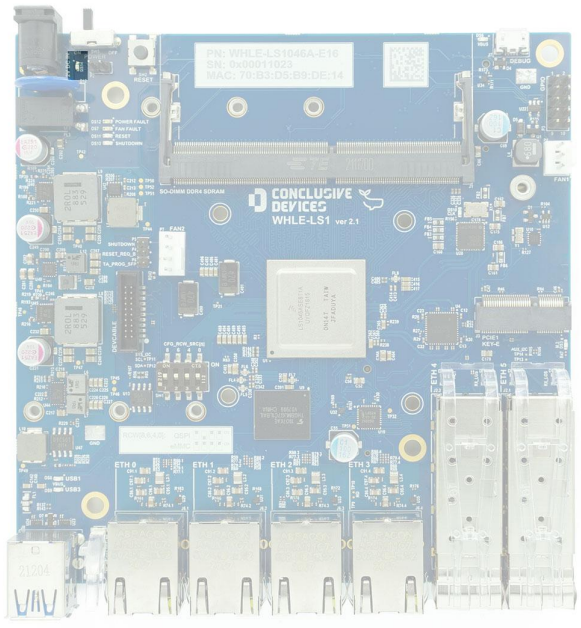
6.9. Power switch header



2-pin 2.54mm header. Functionally identical to the main power switch. When shorted it overrides the power switch, keeping the board in ON state regardless of the power switch position.

WARNING: The power switch and the power switch header behaves as logical OR. Power ON is the dominant state.

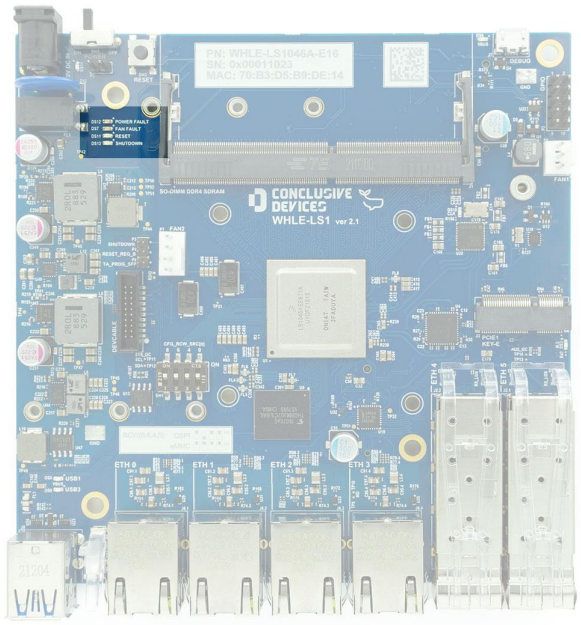
6.10. LED power supply voltage indicator



Green color LED indicating presence of 12V power supply to the board.

The LED lights up when there is voltage present on the VIN- pin of Texas Instruments INA220A power monitoring IC.

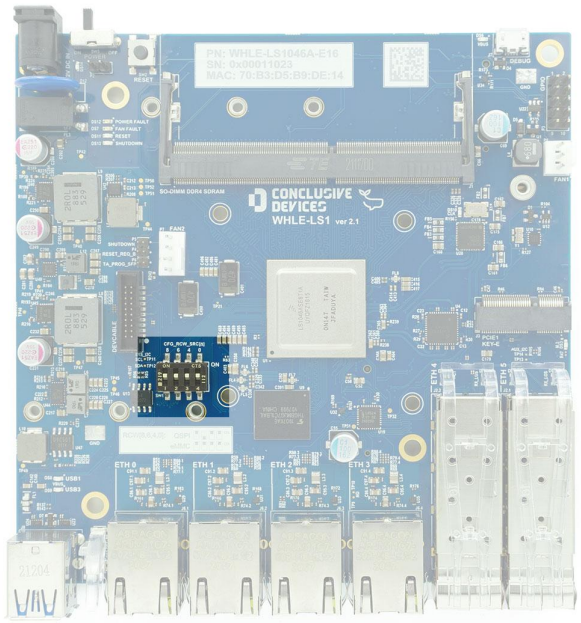
6.11. LED Board States



LED Group indicating board states:

- Power Fault (Red). Lights up when there's an issue on any of the board's power rails, with the exception of the board's main 12V power supply.
- Fan Fault (Red). Lights up when fans controller unit reports alert.
- Reset (Yellow). Lights up when the SoC performs a soft reset of the board (HRESET_B is asserted).
- Shutdown (Yellow). Lights up when the SoC is in the shutdown state. To wake from shutdown, perform a full power cycle, or press the reset button.

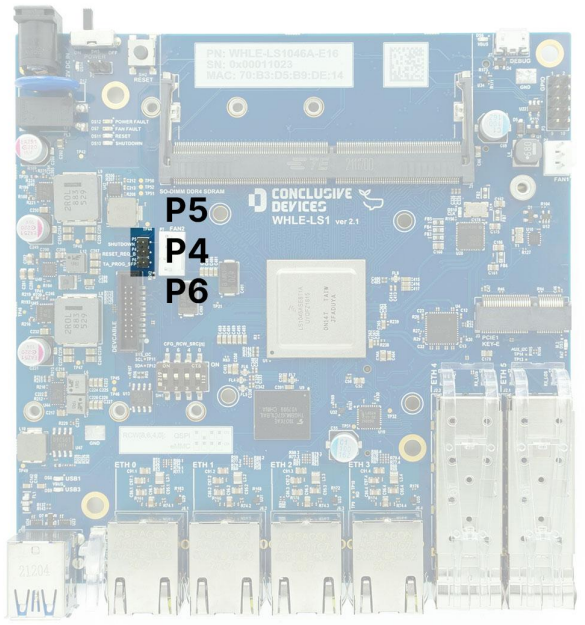
6.12. DIP switch for power boot selection



4 position DIP switch for boot source selection (QSPI Flash or eMMC).

For DIP switch configuration please refer to the **Boot process and provisioning** section of this document.

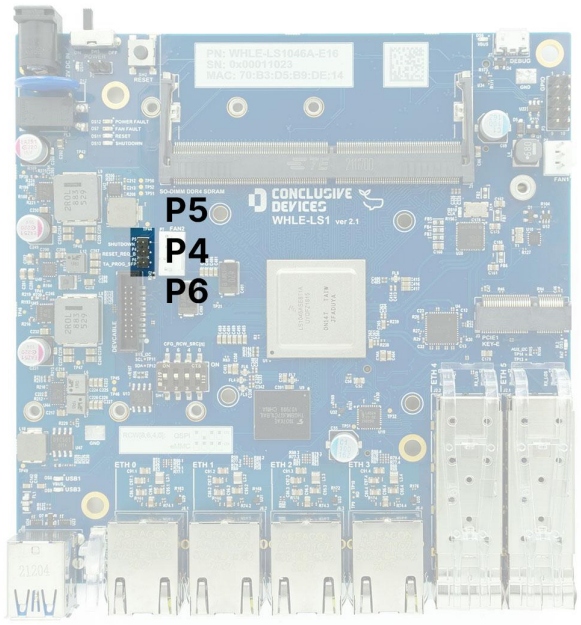
6.13. SHUTDOWN header



2-pin 1.27mm header (P5).

Breaking this header disables the SoC's shutdown capability.

6.14. RESET_REQ_B header

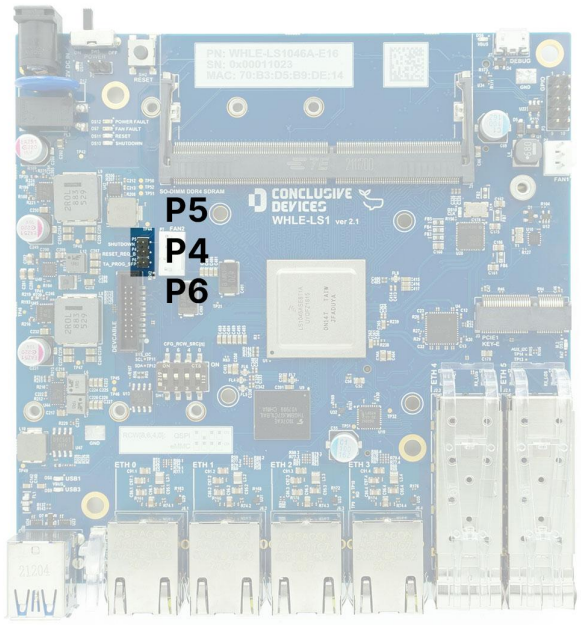


2-pin 1.27mm header (P4).

WARNING: During normal operation, this header should always be shorted.

Breaking this header disables the SoC's whole board soft reset capability by disconnecting it from the board's reset tree. This is typically used in board JTAG programming or debugging scenarios, for example when the board becomes stuck in a reset loop.

6.15. TA_PROG_SFP header



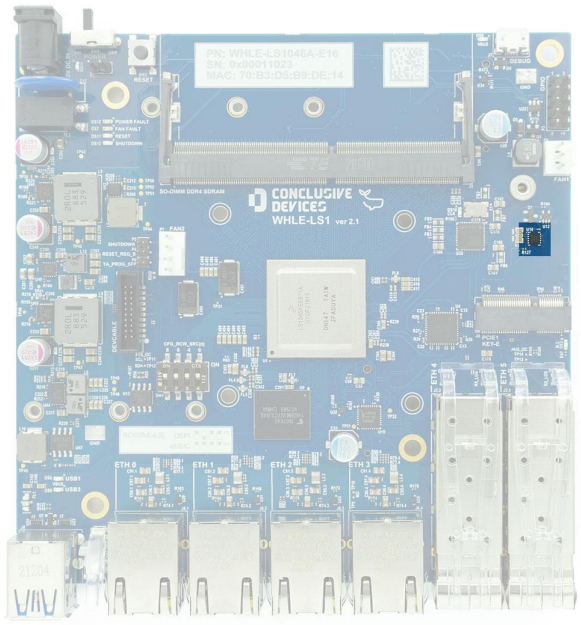
2-pin 1.27mm header (P6).

WARNING: Pins must not be shorted during normal board operation.

TA_PROG_SFP header is intended for use only during programming of Secure Boot of the WHLE-LS1.

Shorting this header delivers 1.8V to the TA_PROG_SFP pin on the LS1 SoC. This enables Secure Boot configuration via fuse burning on the LS1 SoC.

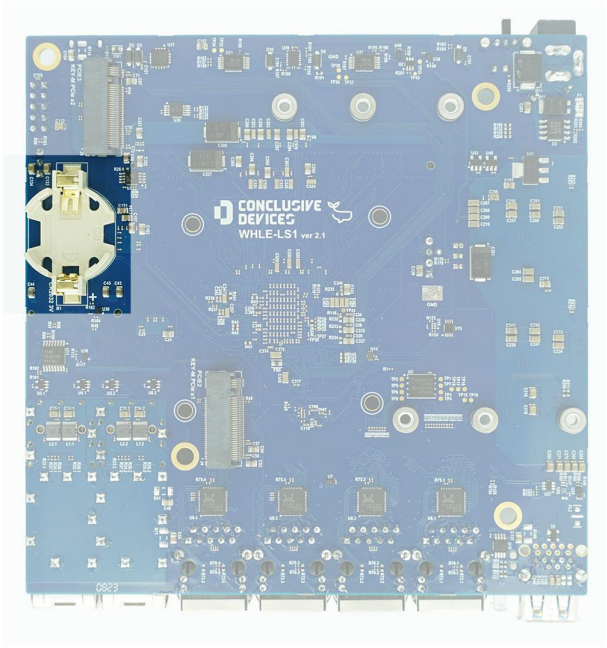
6.16. RTC Clock



NXP PCF85063ATL/1,118 RTC Clock with Calendar:

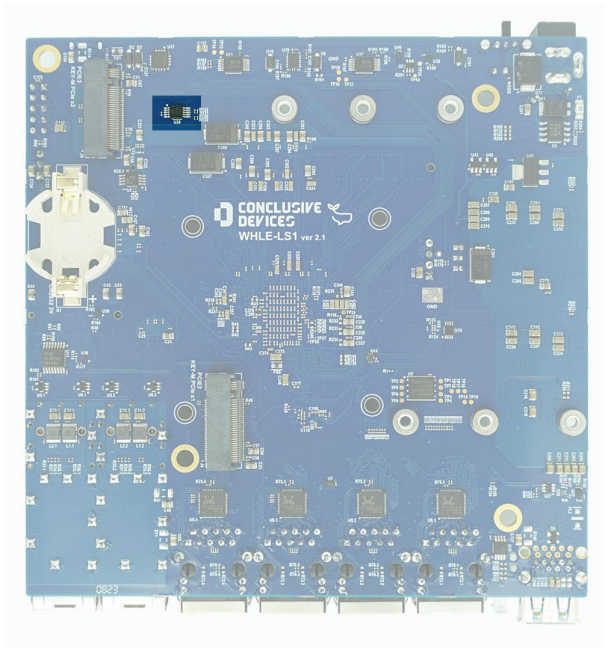
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 0.9 V to 5.5 V
- Low current; typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C
- Alarm function
- Countdown timer
- Minute and half minute interrupt
- Programmable offset register for frequency adjustment

6.17. CR2032 battery slot



One CR2032 battery slot on the back side of the board. It’s connected to the VDD pin of the Real Time Clock throught Schottky barrier diode. Battery’s only function is to supply power to the RTC, and it does not power any other components.

6.18. Fan controller



Microchip EMC2302-1-AIZL-TR fan controller and status monitor. It has 2 PWM-based fan drivers. On WHLE-LS1 it's responsible for controlling both available fan connectors. The fan controller features:

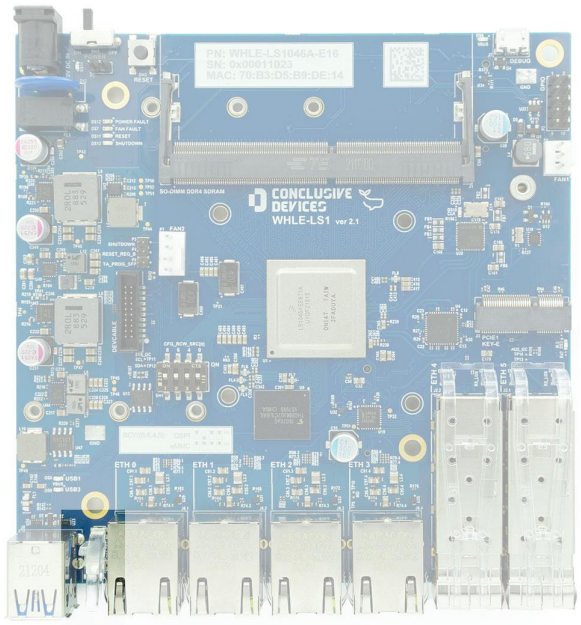
- fan spin up control
- ramp rate control
- fan stall alert
- watchdog timer
- 1% accuracy from 500 to 16000 RPM

The fan controller is available on the board's I2C bus, and fully user programmable. In the default WHLE-LS1 configuration, the fan controller:

- is not programmed
- has the watchdog function turned on, and is expecting I2C communication within 4 seconds of receiving power.
- if no communication over I2C happens, the controller turns on all installed fans to 100%, and turns on the **LED Fan Fault**.

The fan controller's alert pin is connected to the **LED Fan Fault**, and to the board's GPIO expander.

6.19. LED User-Programmable



Two bi-color green/red LEDs with a light pipe. User-programmable, can be used to display status, error codes, etc.

They are connected to an NXP PCA9633DP1,118 - bi-color LED driver which is present as an addressable device on the system's I2C bus.

7. Configuration

7.1. SerDes lane assignments

WHLE-LS1 series offers two SerDes modules (SerDes1 and SerDes2), each having four lanes supporting up to 10.3125Gbit/s speeds.

Table 7.1 SerDes 1 Lanes

Lane	Function
SD1_0	SFP+ interface (10.3125 Gbit/s)
SD1_1	SFP+ interface (10.3135 Gbit/s)
SD1_2	SGMII interface (1.25 Gbit/s)
SD1_3	SGMII interface (1.25 Gbit/s)

Table 7.2 SerDes 2 Lanes

Lane	Function
SD2_0	PCIe x1 (Gen3) connected to a M.2 Key-E slot (2.5/5/8Gbit/s)
SD2_1	PCIe x1 (Gen3) connected to a M.2 Key-M slot (2.5/5/8Gbit/s)
SD2_2	PCIe x2 (Gen3) connected to a M.2 Key-E slot (2.5/5/8Gbit/s)
SD2_3	Complementary to PCIe on SD2_2

7.2. I2C peripherals

7.2.1. SYS_I2C (I2C1)

Table 7.3 SYS_I2C address table

Address	Peripheral
0x03	Led controller (soft reset)
0x09	Clocks generator
0x18	XFI retimer
0x22	IO expander
0x2E	Fan controller
0x50	SODIMM DDR4 slot
0x51	RTC
0x56	64kb EEPROM
0x62	LED controller
0x70	LED controller (all call)

7.2.2. AUX_I2C (I2C3)

Table 7.4 AUX_I2C address table

Address	Peripheral	
0x70	I2C multiplexer	
0x–	Channel 0	PCIe M.2 x1 Key-E slot
0x50/0x51	Channel 1	SFP+ 1 connector
0x50/0x51	Channel 2	SFP+ 2 connector

Address	Peripheral	
0x–	Channel 3	GPIO header connector

7.3. UART configuration

7.3.1. DEBUG_UART (UART1)

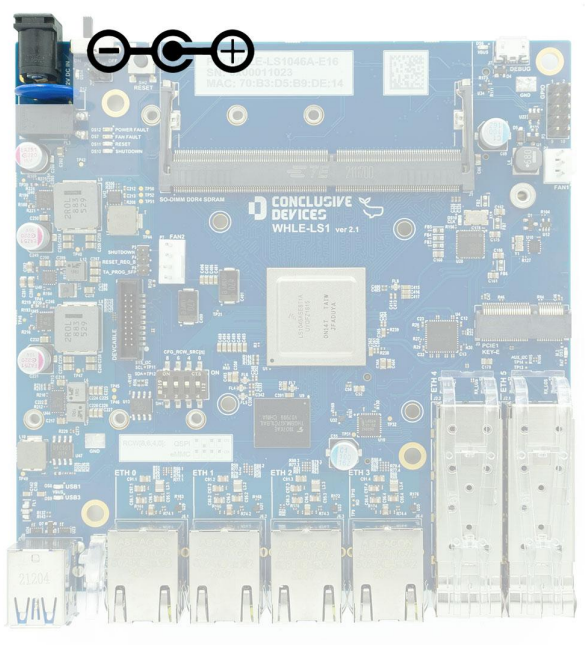
Debug/console UART available on the microUSB connector via the FTDI FT230XQ-R USB to Basic Serial UART IC. It can be switched to expose the UART on the Conclusive Developer Cable connector instead. Switching is performed by the GPIO_3 pin on the Developer Cable connector.

7.3.2. PCIE1_UART (UART2)

Connected to the M.2 Key-E PCIe connector.

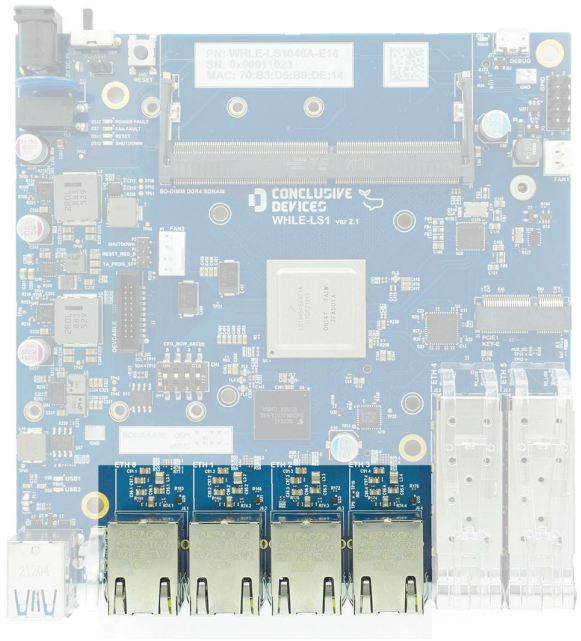
8. External connectors

8.1. Power connector



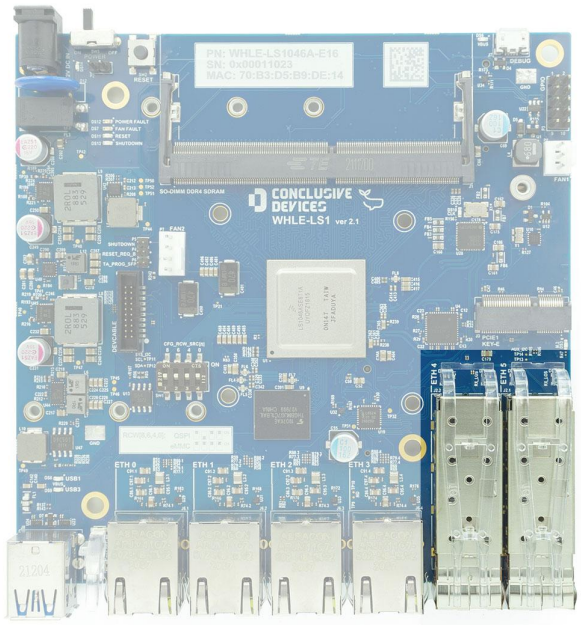
Default board power supply connector, a 12V DC, 2.5x6.5mm female power jack socket, symbol PJ-202BH. Expects a matching male connector with the external contact negative, and the internal contact positive.

8.2. Ethernet RJ-45 connectors



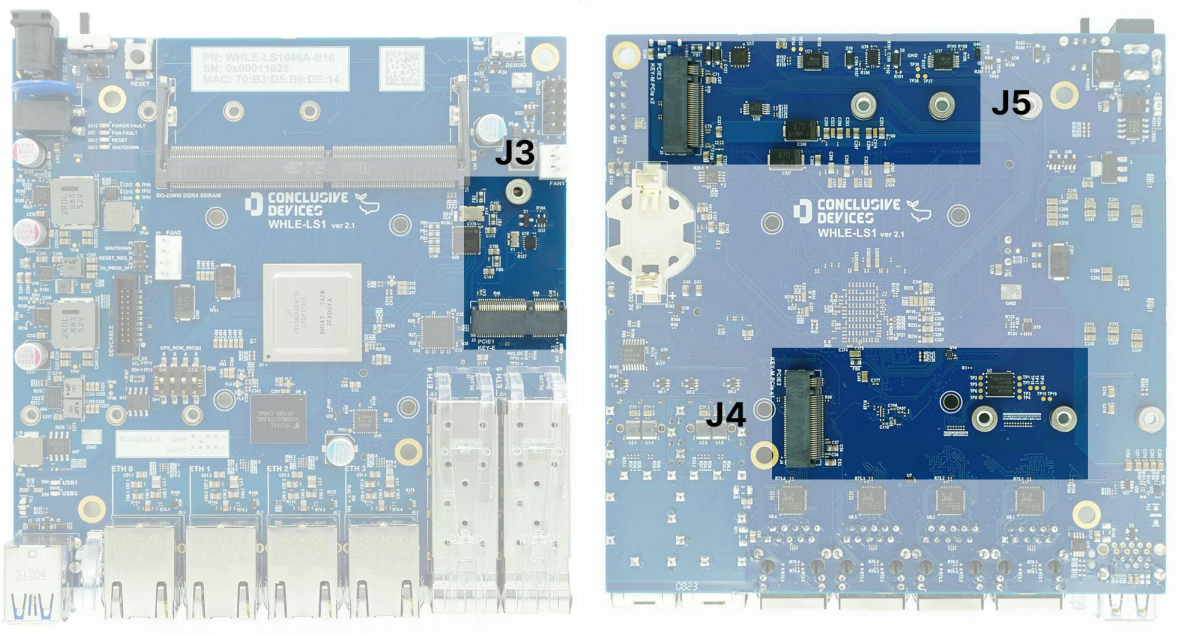
Four RJ45 connectors with LED status indicators. Each is capable of 10/100/1000 Mbit/s bandwidth, and each of the ports is controlled by a Realtek RTL8211FS-CG PHY oriented on the back side of the board.

8.3. SFP+ connectors



Two SFP+ connectors. Each is capable of 1000/10000 Mbit/s bandwidth. LED indicators are implemented via plastic light guides that overlay the SFP+ connector. They are transmitting light from SMD LEDs mounted directly on board. The LEDs are a part of the SFP+ circuit, and are not user-accessible.

8.4. M.2 PCIe slots

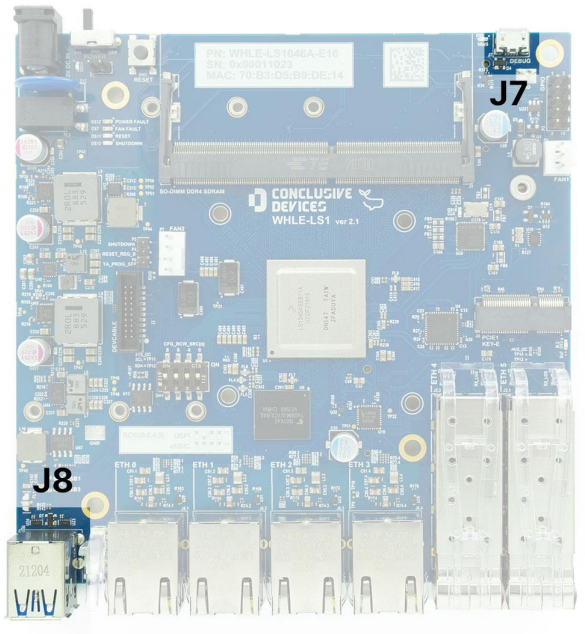


M.2 PCIe slots:

- Key-E 1x PCIe 3.0 slot (J3),
- Key-M 1x PCIe 3.0 slot (J4),
- Key-M 2x PCIe 3.0 slot (J5).

Key-E is intended for a wireless card or an expansion module, but apart from its dimensions it is functionally identical to Key-M slots. For storage purposes, the PCIe slots support NVMe SSDs. SATA SSDs are not supported. M.2 SATA controllers and other PCIe devices should be supported, but may require additional drivers or other modifications. In case of issues with M.2 devices, please contact us.

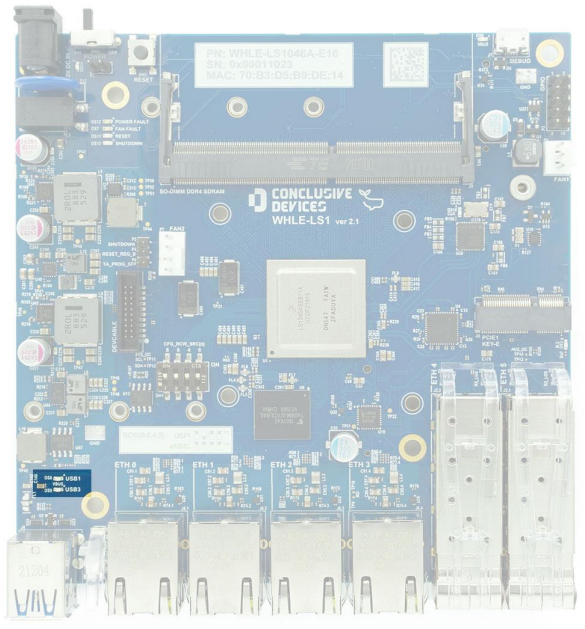
8.5. USB connectors



USB connectors:

- Two (LS10x6) or one (LS10x8) USB 3.0 Type-A ports (J8).
- One USB 2.0 Micro-B port for DEBUG_UART via FT230X (J7).

8.6. LED USB 3.0 Status

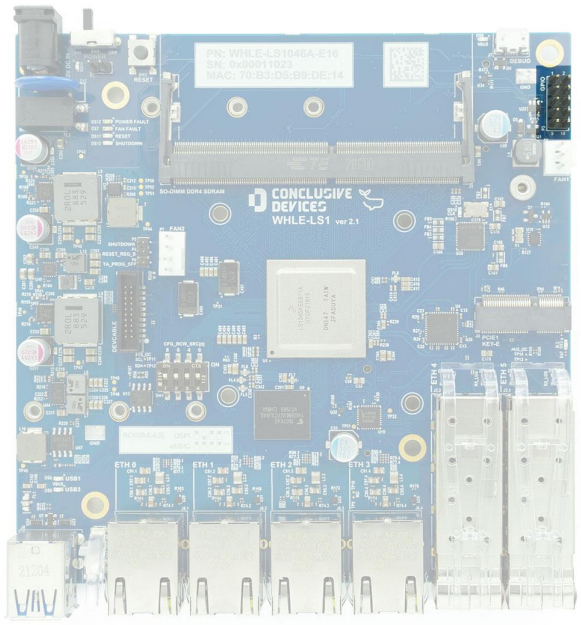


Green color LEDs. They indicate USB port activity.

WHLE-LS1 comes with one or two USB ports, depending on the SoC. When two ports are present, they are stacked vertically.

USB1 LED indicates activity on the lower port, that's present regardless of WHLE-LS1 variant. USB3 LED indicates activity of the upper port, if present.

8.7. GPIO header

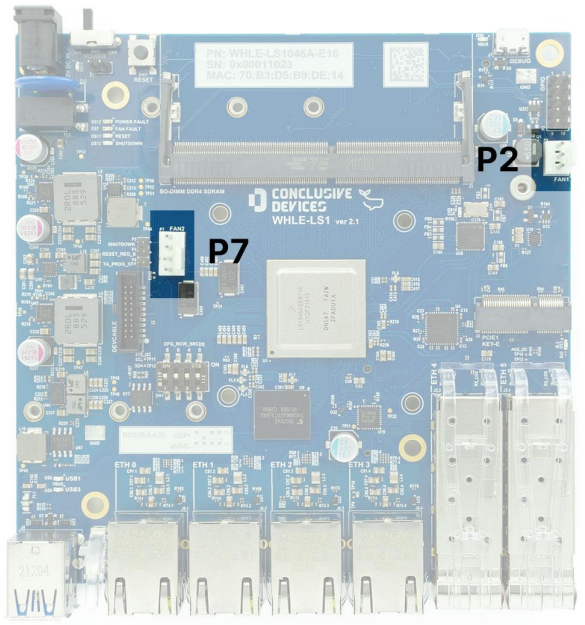


General purpose header. Contains power output, six GPIO lanes and an I2C interface.

Table 8.1 General purpose header pinout

Pin	Pin name	Direction	Description
1	VCC_3V3	Power	3.3V provided by the board
2	GND	Power	Ground
3	GPIO0	In/Out	General purpose input-output, connected directly to CPU
4	GPIO1	In/Out	General purpose input-output, connected directly to CPU
5	GPIO2	In/Out	General purpose input-output, connected directly to CPU
6	GPIO3	In/Out	General purpose input-output, connected directly to CPU
7	GPIO4	In/Out	General purpose input-output, connected directly to CPU
8	GPIO5	In/Out	General purpose input-output, connected directly to CPU
9	SCL	Out	AUX_I2C clock via multiplexer channel 3, 3.3V
10	SDA	In/Out	AUX_I2C data via multiplexer channel 3, 3.3V

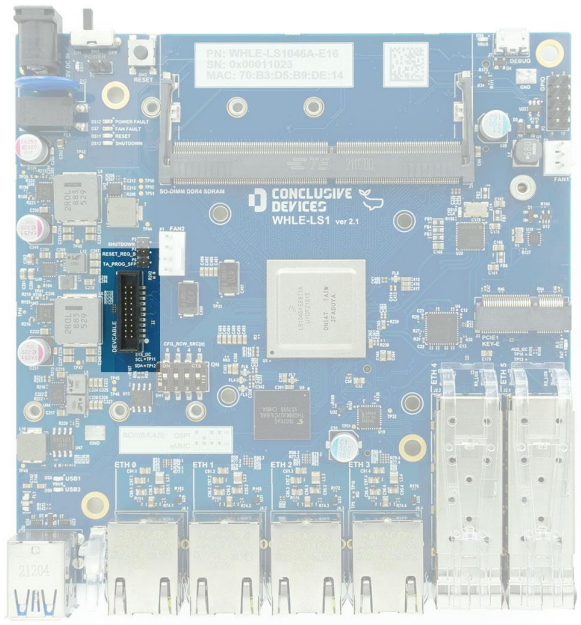
8.8. Fan connectors



- One 3-pin 2.54mm standard fan connector (P2),
- One 4-pin 2.54mm standard fan connector (P6).

Both are controlled via the Microchip EMC2302-1-AIZL-TR fan controller.

8.9. Developer cable connector



Conclusive Developer Cable connector. 20-pin 1.27mm pitch. Composite header providing access to the following peripherals:

- JTAG (with control signals)
- UART (DEBUG_UART)
- I2C (SYS_I2C)
- EEPROM write protection signal
- Board reset inputs

Pinout:

Table 8.2 Developer Connector Pinout

Pin	Pin name	Direction	Description
1	VCC_IO	Power	Reference I/O voltage provided by the board
2	JTAG_TMS	In	JTAG test mode select
3	GND	Power	Ground
4	JTAG_TCK	In	JTAG clock
5	UART_RXD	Out	DEBUG_UART data receive signal

Pin	Pin name	Direction	Description
6	JTAG_TDO	Out	JTAG data output
7	UART_TXD	In	DEBUG_UART data transmit signal
8	JTAG_TDI	In	JTAG data input
9	JTAG_nTRST	In	JTAG test reset (active low)
10	JTAG_nRESET	In	JTAG reset (active low)
11	I2C_SCL	In/Out	SYS_I2C clock
12	JTAG_BSR_VSEL	In	An IEEE 1149.1 JTAG Compliance Enable
13	I2C_SDA	In/Out	SYS_I2C data
14	JTAG_TBSCAN_EN	In	An IEEE 1149.1 JTAG Compliance Enable
15	EEPROM_WP	In	EEPROM write protection (active low)
16	DEBUG_UART_MUX	In	Switch DEBUG_UART between Developer cable connector and Micro-B USB port
17	MASTER_RESET_N	In	Reset input equal to the reset button (active low)
18	GND	Power	Ground
19	GND	Power	Ground
20	GND	Power	Ground

9. Electrical specifications

9.1. Absolute maximum ratings

Table 9.1 Absolute maximum ratings

Characteristic	Max Value	Unit
Max Platform Supply Voltage	15	V

9.2. Recommended operating conditions

Table 9.2 Recommended operating conditions

Characteristic	Recommended Value	Unit
Platform Supply Voltage	12	V

9.3. Power consumption

Average power consumption in idle state: 6-8 Watts.

Maximum power consumption: 72W

9.4. Recommended power supply:

WHLE-LS1 typically comes with a matching power supply. In case a power supply is not available, please use a matching 12V power supply capable of delivering at least 6A, with a matching connector as described in the **Power connector** section.

10. Environmental Specifications

Table 10.1 Environmental specification

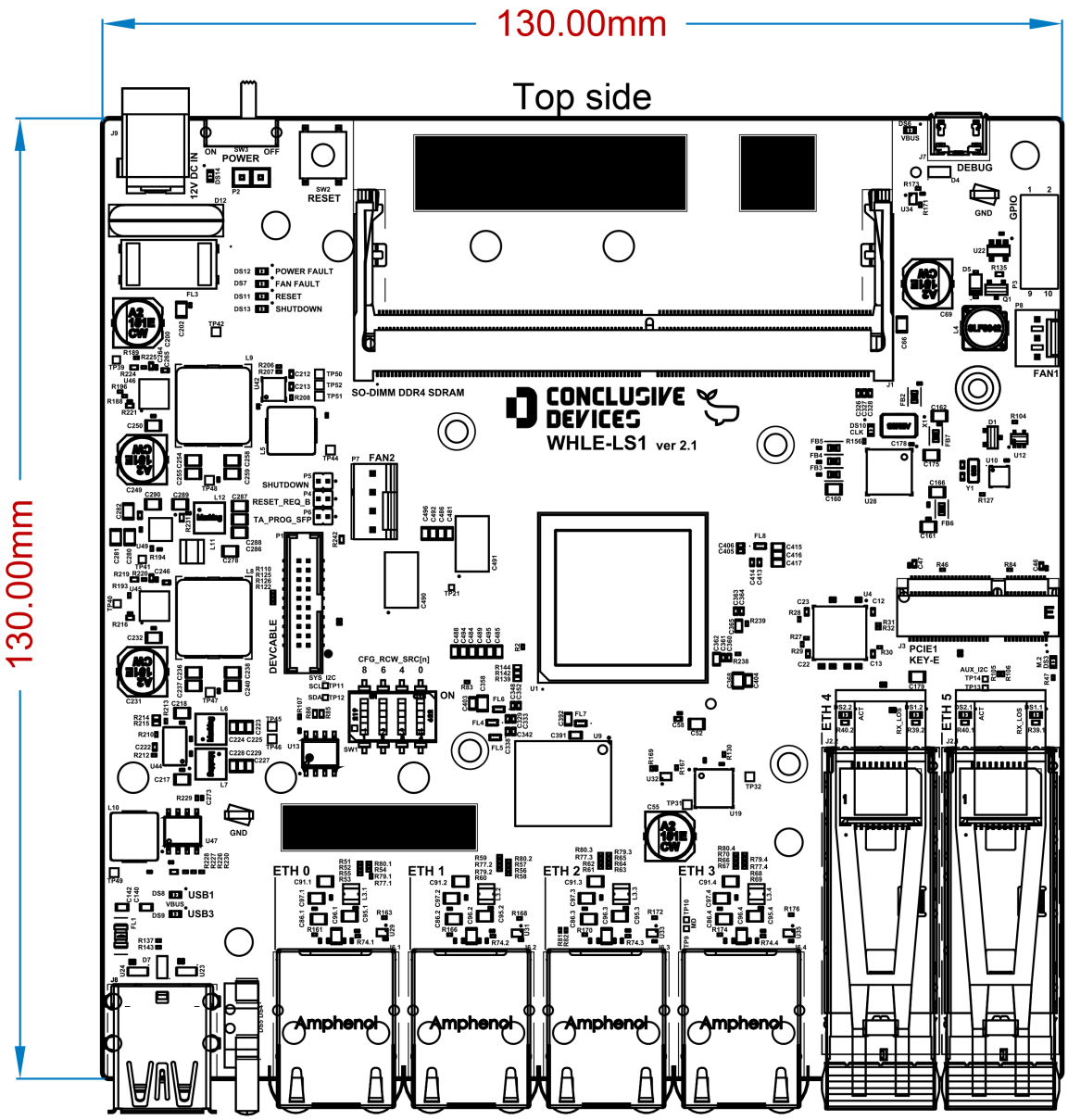
Parameter	Min	Max
Operating temperature range	0°C	+85°C
Storage Temperature	-60°C	+120°C
SoC Junction temperature	0°C	+85°C

WARNING: System with an installed CR2032 battery must not exceed the temperature range of 0°C to +30°C at any time due to battery temperature limits.

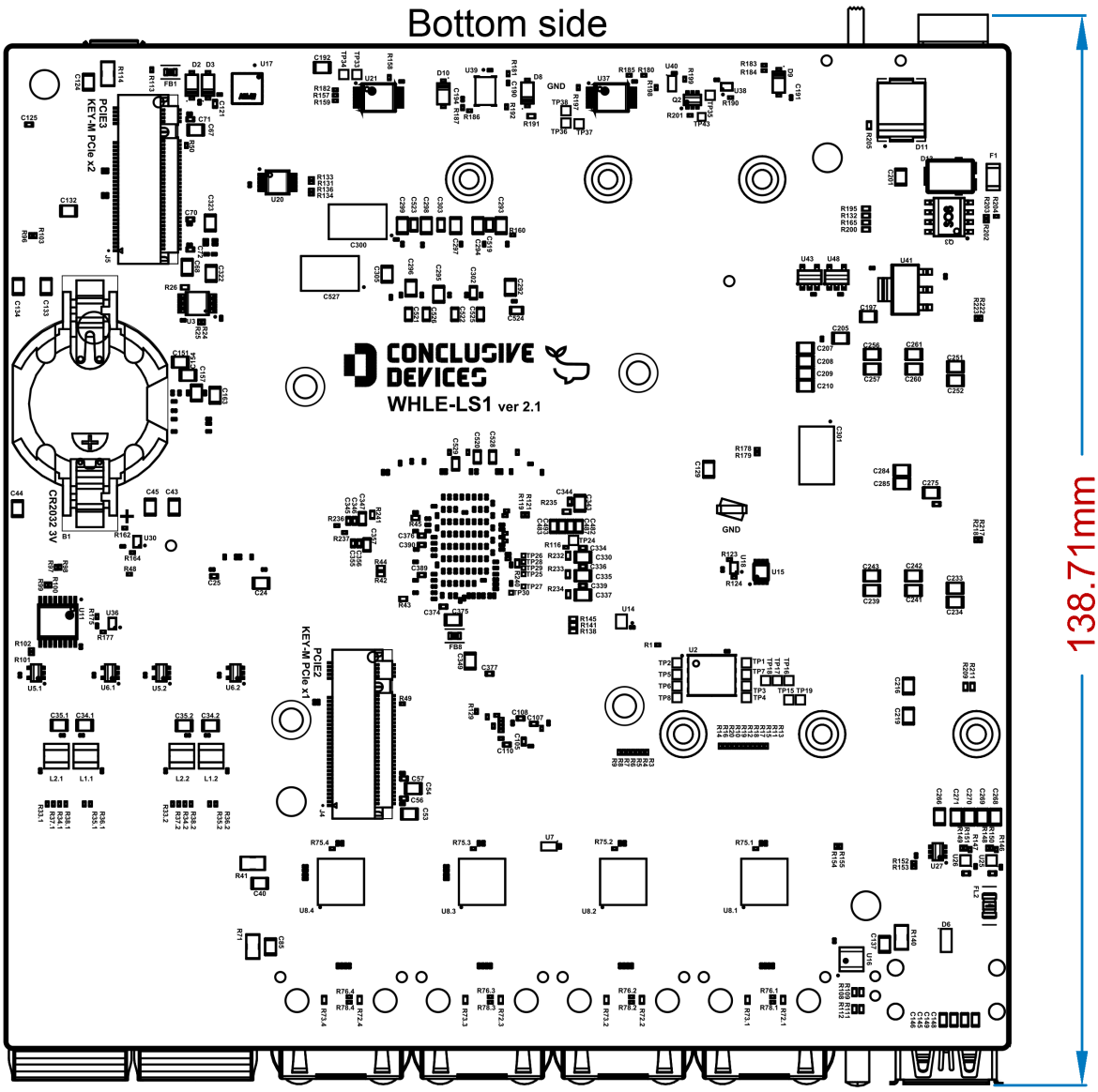
To exceed this limit, please remove or change the CR2032 battery to one certified for target temperature use

11. Mechanical drawings

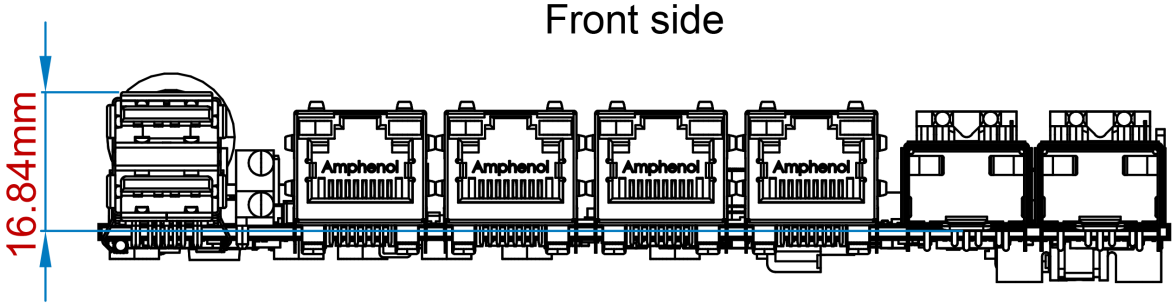
11.1. Mechanical drawings

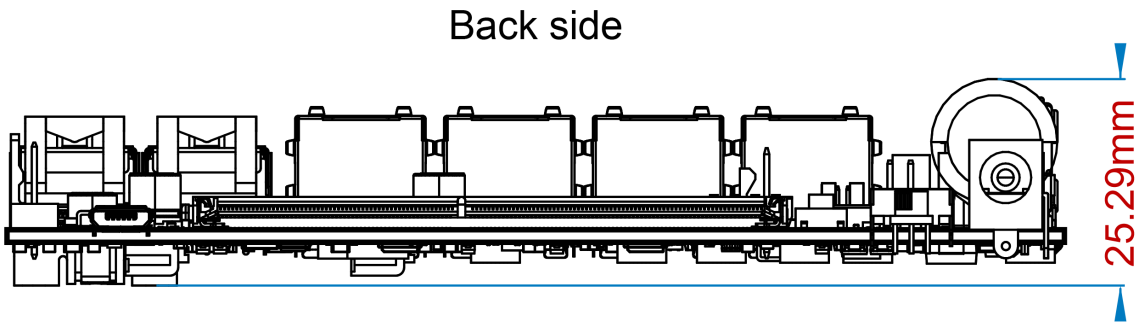


Bottom side



Front side

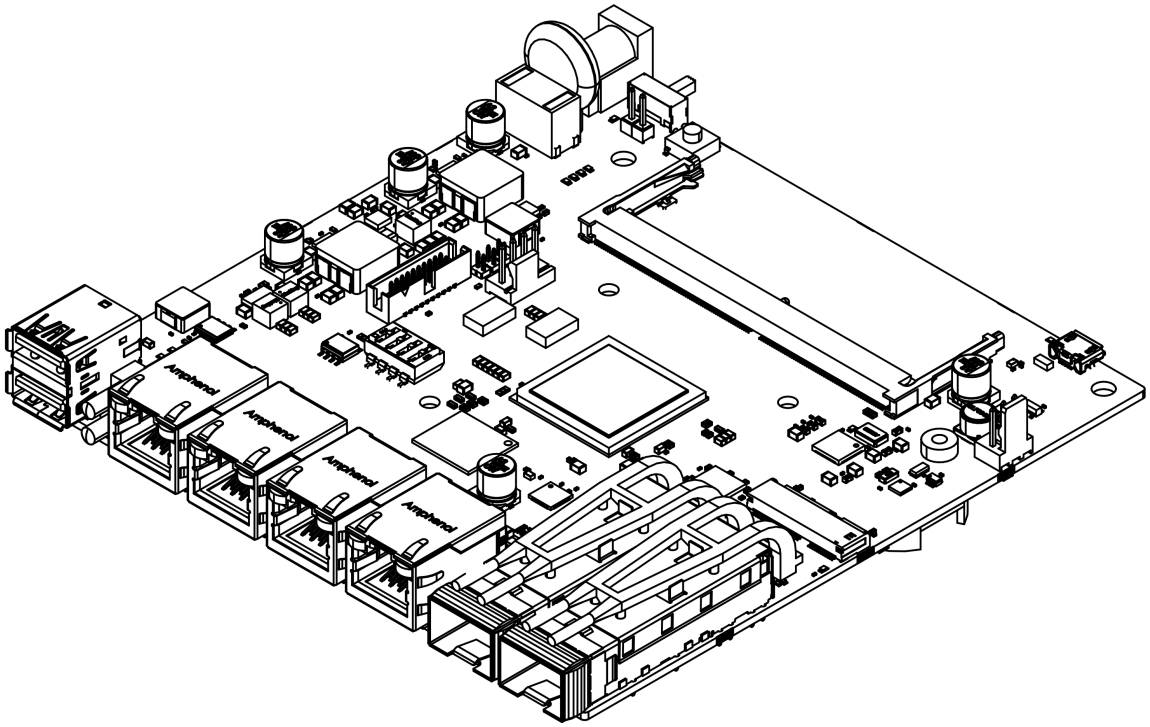




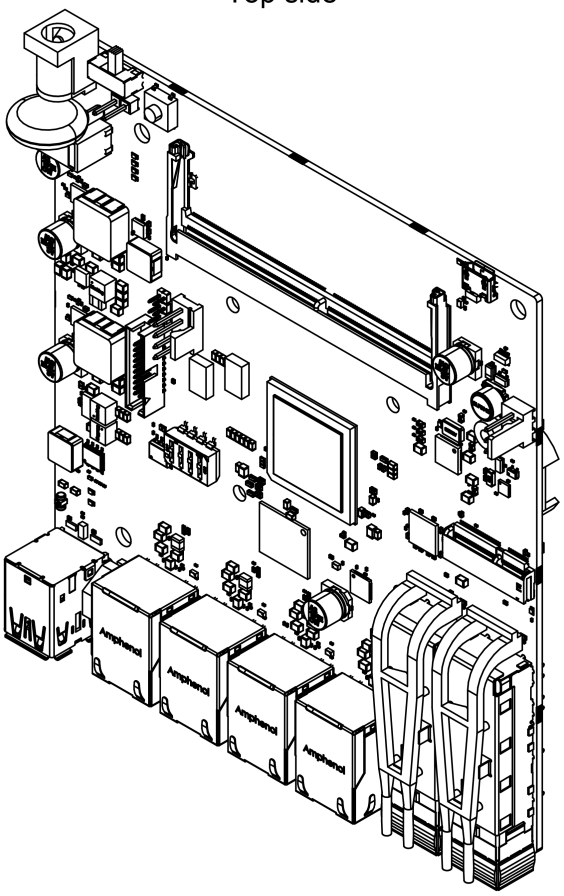
- Overall height with included heatsink and cooling fan: 34mm

11.2. Isometric drawings

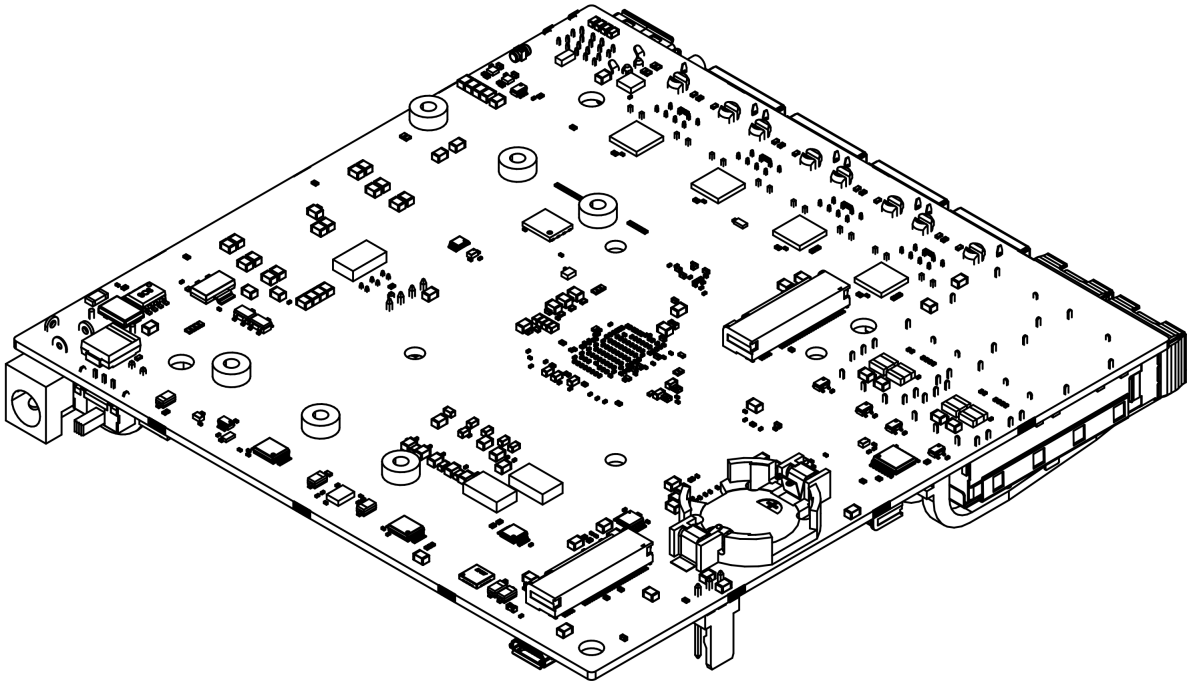
Front side



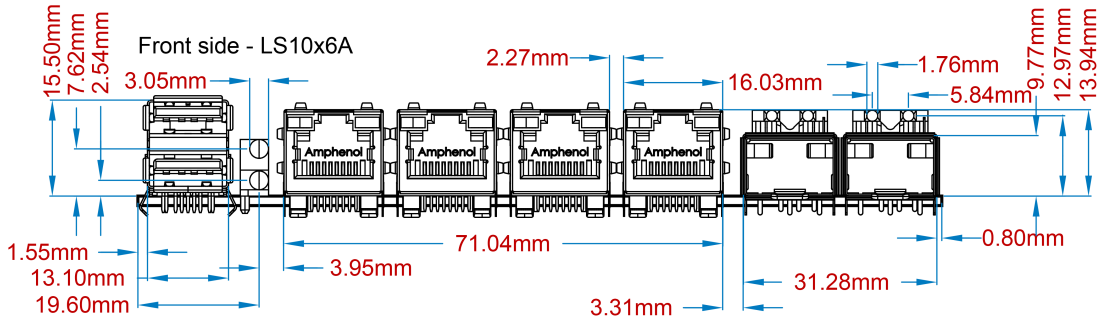
Top side

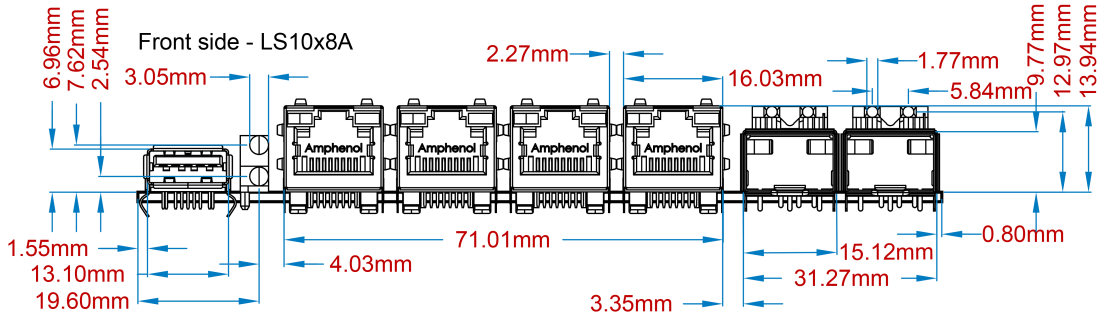


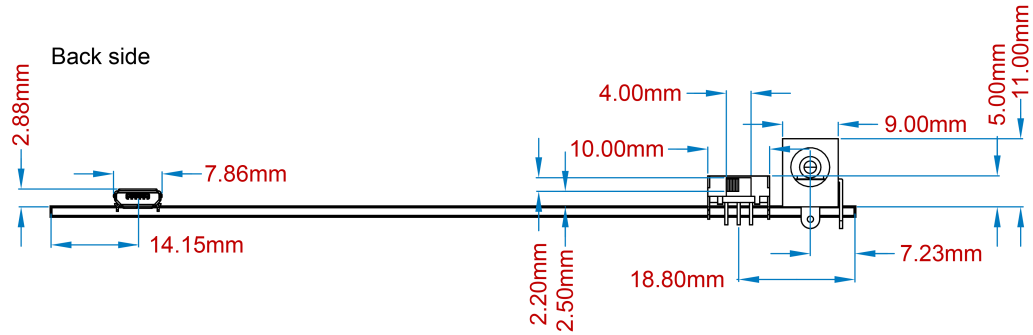
Back side

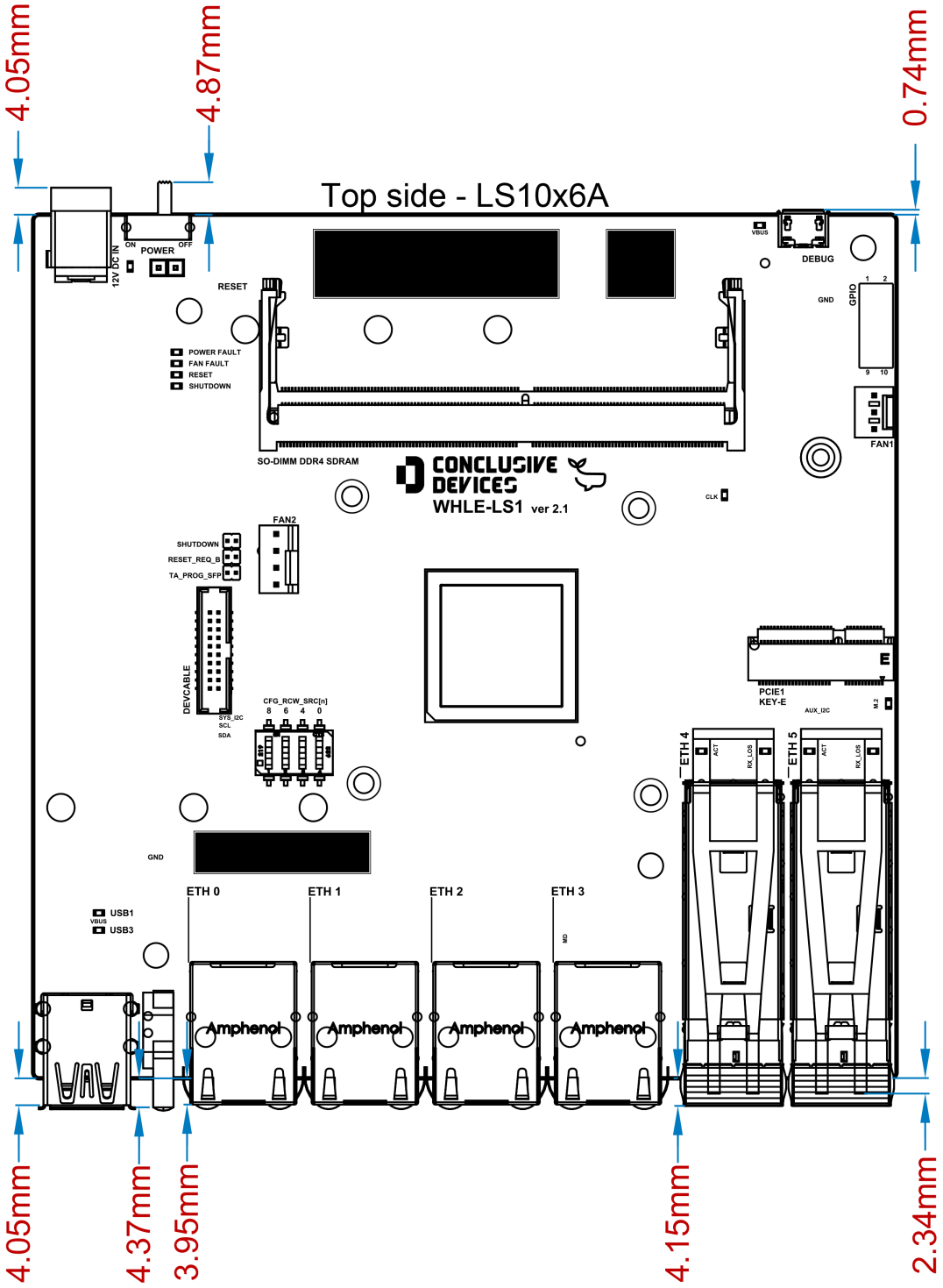


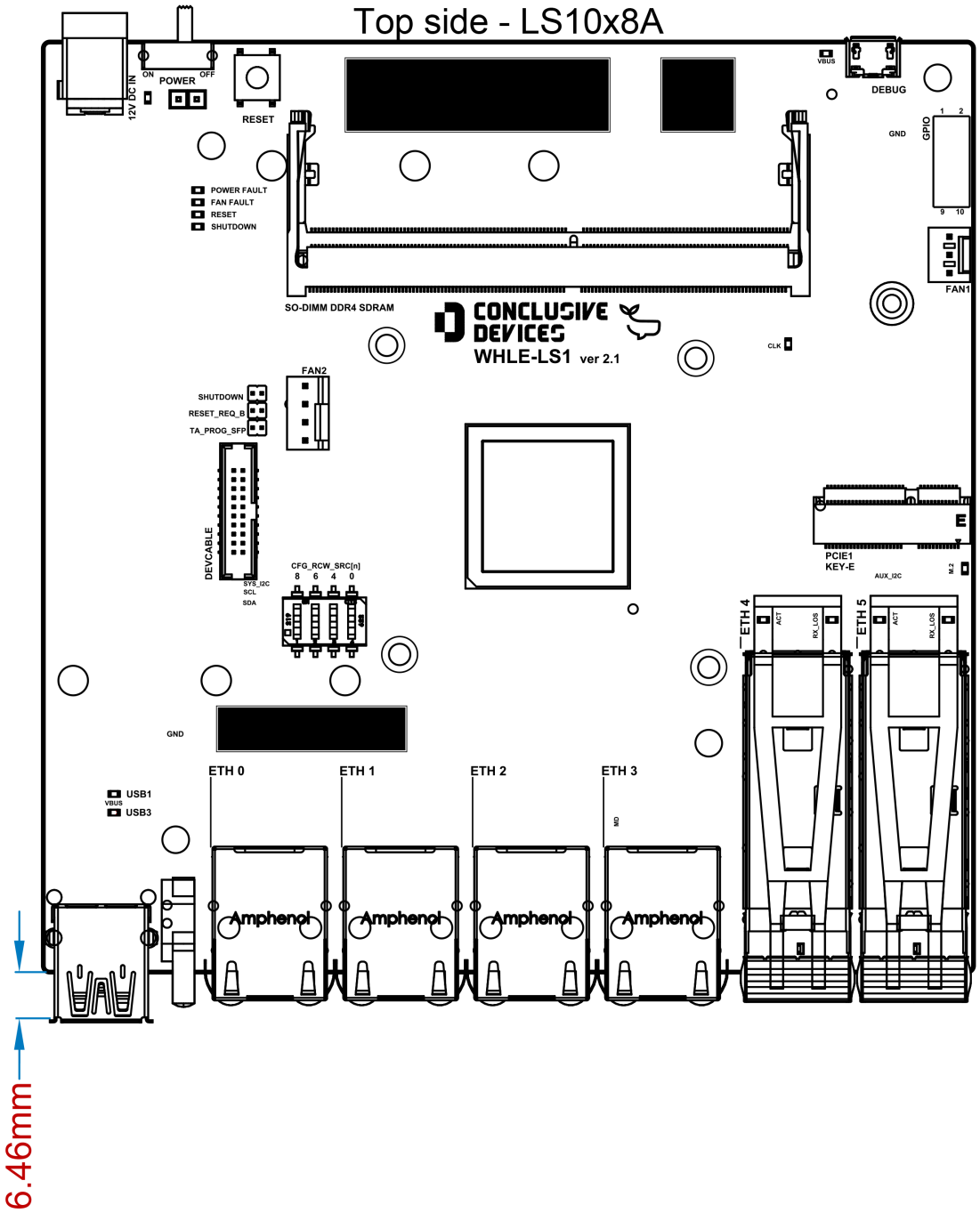
11.3. Dimmensions drawings

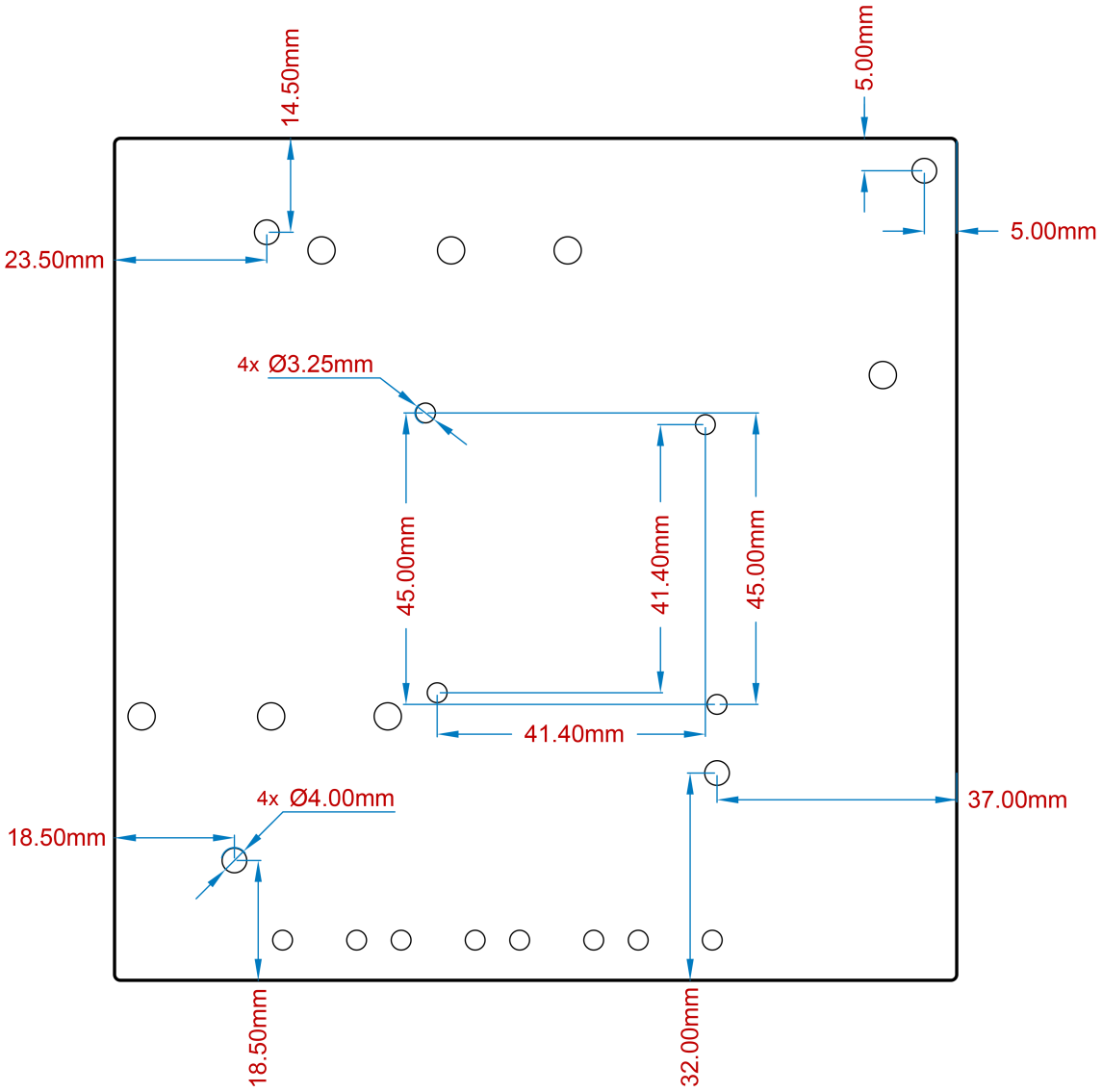







4.05mm
4.87mm
0.74mm
Top side - LS10x6A
12V DC IN
ON
POWER
OFF
RESET
POWER FAULT
FAN FAULT
RESET
SHUTDOWN
VBUS
DEBUG
GND
GPIO
FAN1
SO-DIMM DDR4 SDRAM
CONCLUSIVE DEVICES
WHLE-LS1 ver 2.1
CLK
FAN2
SHUTDOWN
RESET_REQ_B
TA_PROG_SFP
DEVCABLE
SYS_I2C
SCL
SDA
CFG_RCW_SRC[n]
8 6 4 0
PCIE1
KEY-E
AUX_I2C
M.2
ETH 4
ETH 5
ACT
RX_LOS
GND
ETH 0
ETH 1
ETH 2
ETH 3
MD
USB1
VBUS
USB3
Amphenol
4.05mm
4.37mm
3.95mm
4.15mm
2.34mm


Top side - LS10x8A
12V DC IN
ON
POWER
OFF
RESET
POWER FAULT
FAN FAULT
RESET
SHUTDOWN
SO-DIMM DDR4 SDRAM
CONCLUSIVE DEVICES
WHLE-LS1 ver 2.1
VBUS
DEBUG
GND
GPIO
FAN1
CLK
FAN2
SHUTDOWN
RESET_REQ_B
TA_PROG_SFP
DEVCABLE
SYS_I2C
SCL
SDA
CFG_RCW_SRC[n]
8 6 4 0
PCIE1
KEY-E
AUX_I2C
M.2
ETH 4
ETH 5
ACT
RX_LOS
GND
ETH 0
ETH 1
ETH 2
ETH 3
MID
USB1
VBUS
USB3
Amphenol
6.46mm


14.50mm
5.00mm
23.50mm
5.00mm
4x Ø3.25mm
45.00mm
41.40mm
45.00mm
41.40mm
4x Ø4.00mm
18.50mm
37.00mm
18.50mm
32.00mm

12. Boot process and provisioning

This chapter describes the possible boot options and the initial device provisioning process. WHLE-LS1 can boot from 3 possible sources:

- eMMC
- QSPI
- JTAG.

12.1. RCW configuration

RCW, the Reset Configuration Word, can be configured by the on-board DIP switch. The DIP switch numbers [1, 2, 3, 4], as marked in the table below, correspond to the bit order of the RCW [8, 6, 4, 2].

Table 12.1 RCW source configuration

CPU	RCW source	Dip switch positions [1,2,3,4]
LS10x6A	eMMC	ON - ON - ON - ON
LS10x6A	QSPI	ON - OFF - ON - ON
LS10x8A	eMMC	ON - ON - ON - OFF
LS10x8A	QSPI	OFF - OFF - ON - ON

13. Ordering information

WHLE-LS1 comes in several variants, with different CPUs and eMMC sizes.

Table 13.1 Part Numbering Nomenclature

Product family	CPU variant	eMMC variant
WHLE	-LS10xxA	-Exx

The available options are:

13.1. CPU variant

Table 13.2 Available CPU variants

CPU variant	CPU part name
-LS1026A	NXP LS1026A SoC, dual core ARM Cortex-A72, DPAA
-LS1046A	NXP LS1046A SoC, quad core ARM Cortex-A72, DPAA
-LS1048A	NXP LS1048A SoC, quad core ARM Cortex-A53, DPAA2
-LS1088A	NXP LS1088A SoC, octa core ARM Cortex-A53, DPAA2

13.2. eMMC memory size

Below are the available options for the integrated eMMC memory.

Table 13.3 eMMC memory size variants

eMMC variant	eMMC size
-E04	4GB
-E16	16GB
-E64	64GB

13.3. Ordering

To place an order, please visit our website at https://store.conclusive.pl or contact us directly.

Build date: 2024-01-17 10:48:14. Release version: b2b1c6e.
Created using Sphinx 7.2.6.